A New Technique for Synthesis of Broad-Band Parametric Amplifiers

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Abstract—A new synthesis technique for providing precise design values for the realization of broad-band parametric amplifiers incorporating practical varactor diode models is presented. The method provides the designer considerable flexibility in choosing the topology of matching networks employed. An integral part of the synthesis scheme is the application of a least-squares optimization procedure which employs exact partial derivatives of the objective function. The partial derivatives are used in the optimization to compute the gain sensitivity of the amplifier with respect to all matching network and diode parameters. For the first time, sensitivity data is presented which quantitatively shows the effect of the device and matching network parameter variations on overall amplifier response. This permits the determination of critical parameters and provides a means for establishing tolerances for various circuit parameters. In comparison with conventional procedures, significantly improved broad-band designs are shown to result.

I. Introduction

PARAMETRIC devices have become increasingly important during the past few years because of their inherent capability to provide low-noise amplification throughout the microwave frequency spectrum. Since its inception, however, the parametric amplifier has been plagued by the problem of having an extremely narrow band response. Numerous researchers have proposed solutions to this problem [1]–[6], [13]. Many techniques, however, neglect the presence of some important varactor diode parasitic parameter or make some simplifying assumption which tends to cause significant discrepancies between predicted and actual responses and parameter values for amplifiers designed to operate over wide (>30 percent) bandwidths. The basis for optimism in solving the problem stems from the belief that by incorporating multiple-resonator matching networks in the amplifier circuitry, broad-band performance is achievable. The work of Seidel and Herrmann [1] was apparently the first attempt to employ multiple tuning to increase bandwidth. However, they considered only the case of degenerate parametric amplifiers and employed an idealized varactor diode model.

Matthaei [2] subsequently developed a somewhat complex procedure which was capable of providing nondegenerate parametric amplifiers with perhaps 10 percent fractional bandwidths (for gains of 15 dB); however, there is no direct way given for choosing the proper resonators.

Perhaps the most widely used technique to date is that developed by DeJager [5] with extensions by Connors [6]. As was the case with the previous methods, however, this technique, which contains numerous approximations, is limited to the double-tuned signal and single-tuned idler case.

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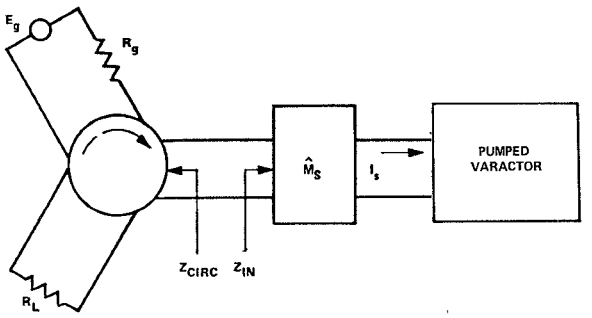

Fig. 1. Parametric amplifier configuration.

This paper is devoted to the development of an exact synthesis technique for providing precise design values for the realization of broad-band parametric amplifiers incorporating practical varactor diode models.

In Section II, the theoretical relations in the fundamental network which are necessary for the development of the synthesis technique are presented. The complete practical realization for the amplifier, including the matching network, is presented, and the network representation to be used in the remainder of the paper is developed.

The synthesis procedure for obtaining the matching networks to be employed in achieving the final design is presented in Section III. Section IV illustrates the entire design procedure, and the synthesis technique is shown to provide excellent results for realization of practical broad-band parametric amplifiers. Also, sensitivity data which quantitatively shows the effect of device and matching network parameter variations on overall amplifier response is presented.

III. Analysis of the Amplifier Configuration

The circuit configuration of the parametric amplifier is shown in Fig. 1. In this figure only signal frequency current is assumed to flow through the signal circuit matching network $\hat{M}_s$. Practical realizations of such amplifiers providing perfect isolation of signal and idler circuits using balanced varactor configurations with single-tuned idlers may be found in the literature [14]–[22].

Employing the usual assumptions for an ideal nonlinear capacitive junction diode, the pump signal magnitude is assumed to be much larger than that of the signal frequency. Consequently, the Fourier series for the nonlinear junction capacitance may be truncated after the fundamental term, and the voltage–current relations for signal and idler circuits may be written as follows:

$$\begin{bmatrix} V_s \\ \overline{V}_i \end{bmatrix} = \begin{bmatrix} \dfrac{1}{C_0 j\omega_s} & \dfrac{-1}{C_1 j\omega_i} \\ \dfrac{1}{C_1 j\omega_s} & \dfrac{-1}{C_0 j\omega_i} \end{bmatrix} \begin{bmatrix} I_s \\ \overline{I}_i \end{bmatrix}$$

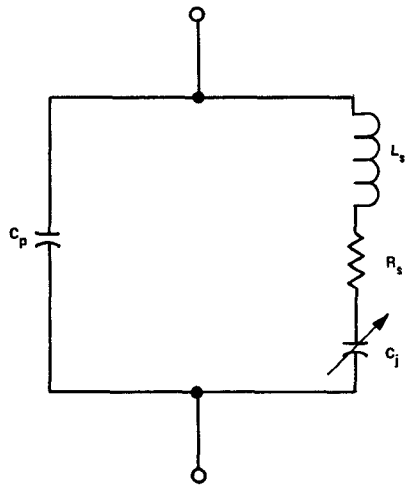

Fig. 2. Varactor diode model.

where C_0 and C_1 represent the terms in the truncated expansion for the nonlinear junction capacitance,[1] the s and i subscripts represent signal and idler quantities, respectively, and the bar — denotes complex conjugation.

The equivalent circuit for the packaged varactor diode is shown in Fig. 2. In this figure, C_p represents the parasitic capacitance due to the encapsulation surrounding the semiconductor junction, L_s represents the parasitic inductance arising from the lead wire, C_j is the junction capacitance which is a nonlinear function of the applied voltage, and R_s is a resistance representing diode losses.

Employing the equivalent circuit (Fig. 2) for the varactor diode in the general amplifier configuration and recalling that the pump circuit does not enter directly into the analysis, a new equivalent circuit may be drawn as shown in Fig. 3 [14], [17], [18], [20]. Note that the circulator has been replaced by its Thevenin equivalent circuit.

The impedance Z_s in Fig. 3 is given by

$$Z_s = \frac{1}{j\omega_s C_0} - \frac{1}{\omega_s \omega_i C_1^2 Z_{ii}} \tag{1a}$$

where

$$Z_{ii} = R_{ii} + jX_{ii} \tag{1b}$$

$$R_{ii} = R_s + \operatorname{Re} Z_i' \tag{1c}$$

$$X_{ii} = -\left[\operatorname{Im} Z_i' + \left(\omega_i L_s - \frac{1}{\omega_i C_0}\right)\right] \tag{1d}$$

and

$$Z_i' = \hat{Z}_i \Big\| \frac{1}{j\omega_i C_p} \tag{1e}$$

with $\hat{Z}_i$ denoting the idler circuit input impedance[2] and the single-tuned idler assumption being made [16]–[24].

Expressing (1a) in the form

$$Z_s = \frac{1}{j\omega_s C_0} - R(\omega) - jX(\omega)$$

where

$$R(\omega) = \frac{R_{ii}}{\omega_s \omega_i C_1^2 (R_{ii}^2 + X_{ii}^2)} \tag{2}$$

$$X(\omega) = \frac{X_{ii}}{\omega_s \omega_i C_1^2 (R_{ii}^2 + X_{ii}^2)} \tag{3}$$

permits the final circuit for synthesis of matching network $\hat{M}_s$ to be represented as shown in Fig. 4. Note than $\hat{M}_s$ has been augmented by the varactor diode parameters C_o, L_s', and C_p to yield the revised network labeled M_s. The replacement of L_s by an inductance L_s' will be discussed in the next section.

III. Synthesis of the Matching Structure

The design technique proceeds by first synthesizing a preliminary matching network for M_s which is contained within the dotted lines (Fig. 4). It is initially assumed that the impedance $X(\omega)$ [refer to (3)] is negligible, and consequently, the network of Fig. 4 is terminated only in a purely real frequency-dependent negative resistance equal to $-R(\omega)+R_s$. Of course, $X(\omega)$ is identically zero only at the idler circuit resonant frequency; however, it is assumed to be zero only for purposes of a preliminary design. This assumption is completely removed subsequently during the computerized synthesis of the final matching network (see Section III-B).

The mathematical synthesis of the preliminary matching network M_s is based upon an extension of the theory of synthesis of networks for matching resistive generators into resistive loads [7].

The second step in the design process, a computerized synthesis technique, is then employed to obtain the exact network component values for the final design.

A. Analytical Synthesis

Consider the two-port circuit representation of Fig. 4 and assume that the revised matching network M_s has been transformed into an equivalent low-pass structure. The resulting network is redrawn in Fig. 5 where R_2 is taken as the average value of $-R(\omega)+R_s$ over the frequency range of interest.

For moderate to large gain amplifier responses, the assumption is made that s, the reflection coefficient at port 1 [8], will be small, and therefore, the transducer power gain may be written approximately as (see [9])

$$G_T \approx \left|\frac{1}{s}\right|^2.$$

The requisite matching network M_s, to provide a maximally flat response,[3] is then synthesized from port 2 of the circuit of Fig. 5 by employing the standard Darlington approach for prescribed Butterworth response characteristics [7], [10]. When viewed from port 2, the low-pass prototype which results from the revised matching network of Fig. 4 is constrained to have a series inductor as its first element. Consequently, the first element extracted must be a series inductor. Subsequent to the removal of this element, however, a variety

[1] In the literature on nonlinear capacitance diodes, both series and shunt equivalent circuit representations have been used. In this paper, we are employing the series representation so that $C_0/C_1=\alpha$ (see [23, p. 79] or [22]).

[2] In (1), the symbol $\|$ designates a parallel connection.

[3] The best estimate for the maximum bandwidth achievable from a parametric amplifier employing a diode with parasitics for a prescribed gain G_T may be obtained from the relation [4] $G_T \leq \cosh^2 \alpha$, where $\alpha = \pi\sqrt{\omega_{s_0}\omega_{i_0} C_1 (3C_0 - \omega_{s_0}\omega_{i_0} C_1^2 L_s)/(\omega_C^2 L_s C_0^3)}$ and ω_{i_0} and ω_{s_0} are the center frequencies of the idler and signal bands, respectively, and ω_C is the equivalent low-pass bandwidth.

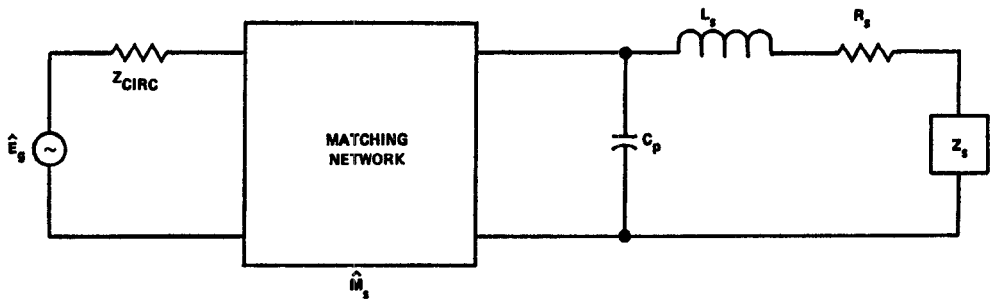

Fig. 3. Revised circuit for analysis where only signal frequency currents are flowing. The idler frequency enters implicitly in the impedance Z_s [see (1a)]

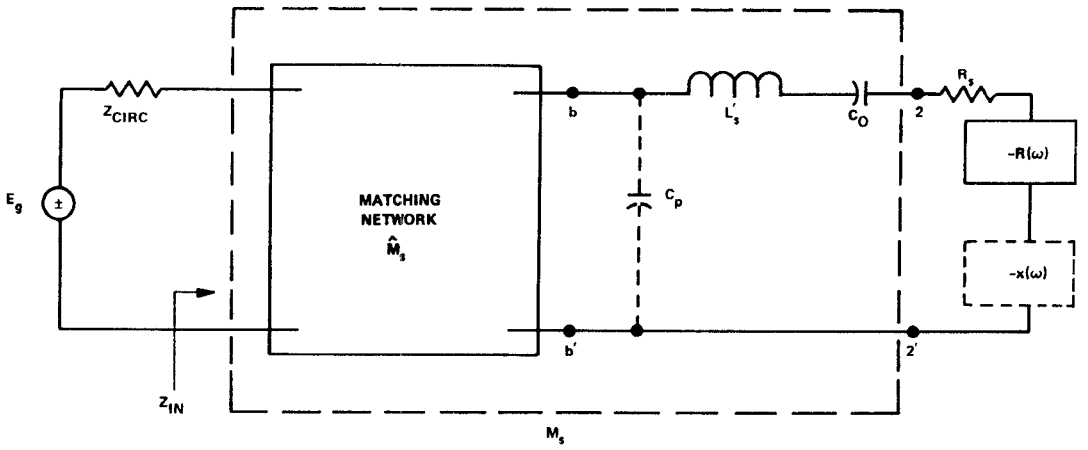

Fig. 4. Revised circuit for synthesis of M_s.

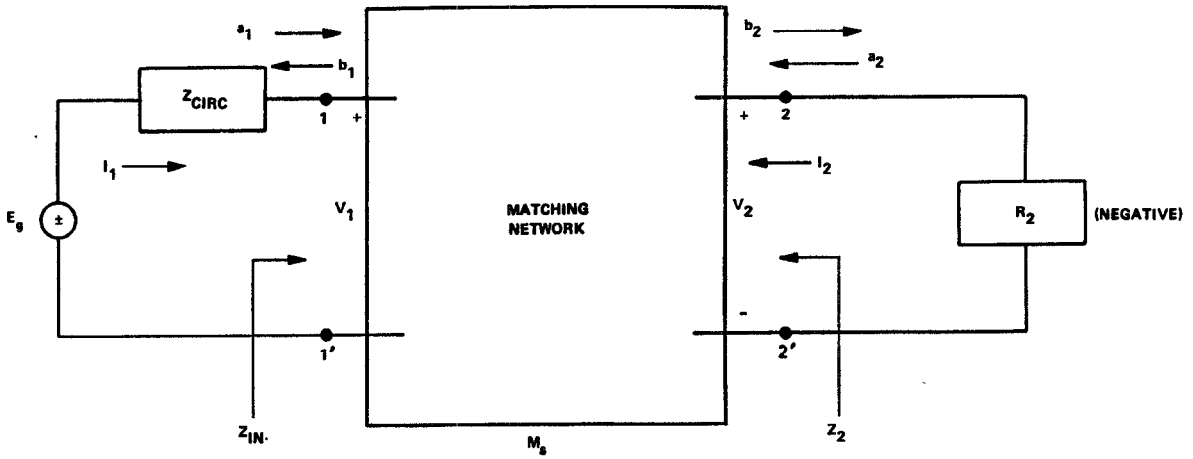

Fig. 5. Fundamental matching problem representation.

of network topologies for M_s are possible.[4] The designer is consequently afforded considerable flexibility in the choice of element location and parameter value. After synthesis of the low-pass prototype, a low-pass to bandpass transformation is performed prior to the application of the computerized synthesis step.

B. Computerized Synthesis

The synthesis technique outlined in the previous paragraph would provide exact parameter values for M_s and a flat amplifier response if the real-part impedance $R(\omega)$ were constant with respect to frequency and $X(\omega)$ were identically zero across the frequency band of interest. As a consequence of the nonuniformity of $R(\omega)$ and the finite value of $X(\omega)$ as revealed by (2) and (3), however, the amplifier transducer power gain response will be expected to deviate from that which was prescribed. To obtain the desired flat response, the element values of M_s must be readjusted accordingly. This is accomplished by application of a least-squares optimization scheme [25]–[27].

The analytical synthesis (Part A) has yielded an overall amplifier design for which an expression for the transducer power gain may be written in terms of frequency and circuit parameters as $G_T = G_T(\omega, \boldsymbol{x})$, where $\boldsymbol{x} = (x_1, \cdots, x_m)$ denotes the vector of adjustable element parameter values. Denoting

[4] It should be noted that for the balanced amplifier realization, all matching network M_s resistors and inductors should be divided by two, and all capacitor values should be doubled [14]–[22].

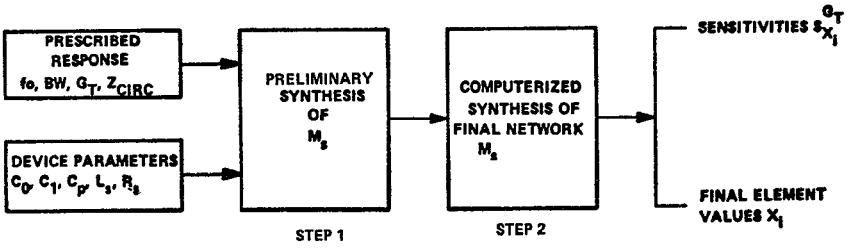

Fig. 6. Block diagram summarizing the steps employed in the design procedure. BW = bandwidth. fo = centerband frequency.

the prescribed amplifier response as $\hat{G}_T(\omega)$, the least-squares objective function ($\hat{O}(\boldsymbol{x})$) takes the form[5]

$$\hat{O}(\boldsymbol{x}) = \langle \boldsymbol{y} - \hat{\boldsymbol{y}}, \boldsymbol{y} - \hat{\boldsymbol{y}} \rangle$$

where

$$\boldsymbol{y} = [G_T(\omega_1, \boldsymbol{x}), \cdots, G_T(\omega_p, \boldsymbol{x})]^T \triangleq G(\boldsymbol{x})$$

and

$$\hat{\boldsymbol{y}} = [\hat{G}_T(\omega_1), \cdots, \hat{G}_T(\omega_p)]^T.$$

The steps employed to obtain an acceptable set of matching network parameters which will provide the desired flat response are as follows.

1) Determine the initial values for the circuit parameters from the analytical synthesis (Part A).

2) Compute the value of the objective function $\hat{O}(\boldsymbol{x})$.

3) Determine whether the magnitude of $\hat{O}(\boldsymbol{x})$ is less than a prescribed value.

4) Iterate the matching network parameters so that the new values minimize the objective function.

5) Repeat steps 2), 3), and 4) until the objective function meets the predetermined value.

C. Additional Remarks

The element values of the bandpass matching network M_s are determined from the standard low-pass to bandpass transformation [10]. However, the value of the first inductor-extracted L_s' necessary to tune the requisite capacitance C_o will be greater than the diode lead inductance L_s. The nature of the analytical expression for the parameters of M_s precludes extraction of the case capacitance C_p at this point. Consequently, this component must be synthesized automatically during the computerized optimization.

The successful implementation of the least-squares optimization scheme requires the evaluation of the partial derivatives of the transducer power gain with respect to the matching network parameter values. This is accomplished by employing a procedure for producing Fortran code expressions for partial derivatives from a basic Fortran model [11]. The computerized synthesis, therefore, employs the exact algebraic partial derivatives of the objective function with respect to the circuit parameters (*including pump frequency*).

The availability of the partial derivatives of the transducer power gain with respect to all parameters of interest provides a means of determining the effects of various circuit parameters on the overall amplifier response. The gain sensitivity, defined by the relation

$$S_{x_i}^{G_T} = \frac{x_i}{G_T} \frac{\partial G_T}{\partial x_i}$$

represents the percentage change in gain for a percentage change in a prescribed circuit parameter x_i. This sensitivity measure permits determination of critical circuit parameters, provides a means for establishing tolerances for various circuit parameters, and re-establishes the importance of precise characterization of the diode and package parameters.

Fig. 6 is a block diagram which summarizes the steps employed in the synthesis procedure. The element values for the matching network M_s, Step 1 of Fig. 6, are determined automatically from closed formulas derived for from 1 to 6 lumped resonators. The lumped resonators are subsequently converted into distributed components using standard techniques [28].

IV. Design Example

To illustrate the efficacy of the design technique, a diode with the following parameter values will be employed:

$C_o = 0.4$ pF
$C_l = 1.6$ pF
$C_p = 0.03$ pF
$L_s = 0.1$ nH
$R_s = 2\ \Omega$

It is desired to synthesize a parametric amplifier with a flat (± 0.25 dB) transducer power gain of 10 dB, a 3 dB bandwidth of 3 GHz, and centerband frequency of 8.0 GHz. For this diode the flat bandwidth predicted by the relations of Kuh [3] or Ku [4] is 5.8 GHz. These theoretical bandwidths exclude the effects of all parasitics and consequently provide optimistic values.

In this example the idler circuit is assumed to be series resonated. Thus, for the preliminary design (Step 1 of Fig. 6), the initial idler frequency was computed to be approximately 25 GHz. It is also assumed for illustrative purposes that the idler is terminated ideally so that the idler load consists o .he diode resistance. Although the use of a physical idler short [14]–[22] may cause degradation of the computed response, when idler frequencies which are several multiples higher than the signal frequency are employed, as was the case in our previous paper [12], the discrepancy is minimal [5]. Alternatively, at lower idler frequencies the computerized synthesis may be employed to provide the exact response once a specific idler termination circuit is prescribed.

Based upon the amplifier response requirements given above, a three-resonator signal circuit matching network is

[5] For two arbitrary $p \times 1$ column vectors $\boldsymbol{w}$ and $\boldsymbol{x}$, the inner product is defined by $\langle \boldsymbol{w}, \boldsymbol{x} \rangle = \sum_{i=1}^{p} w_i x_i^*$.

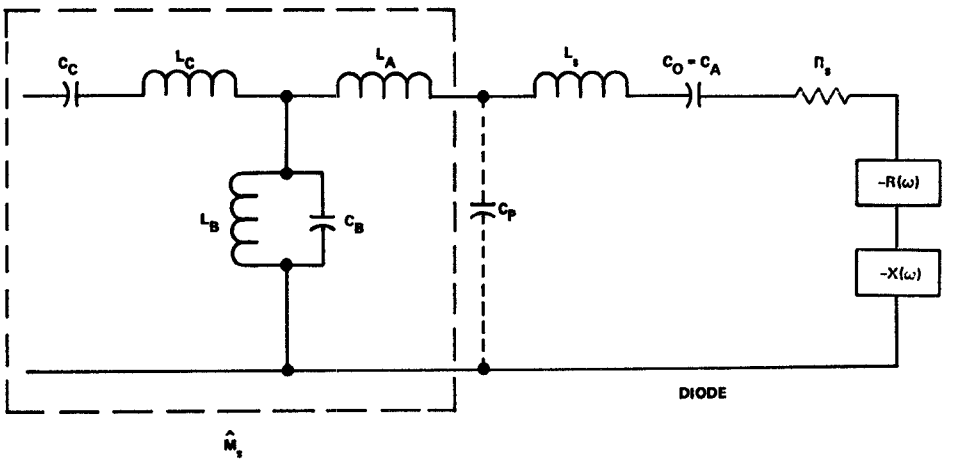

Fig. 7. Parametric amplifier design model.

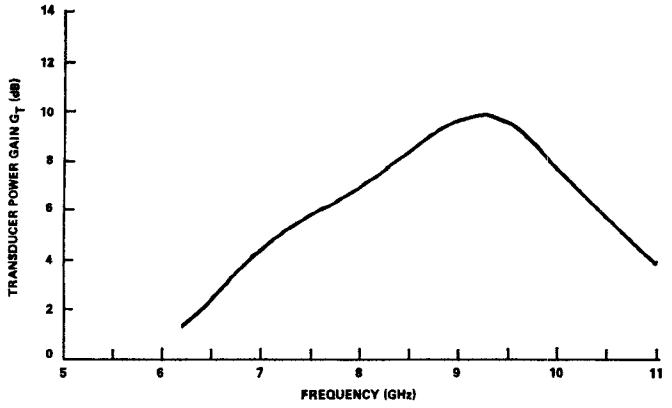

Fig. 8. Initial amplifier response.

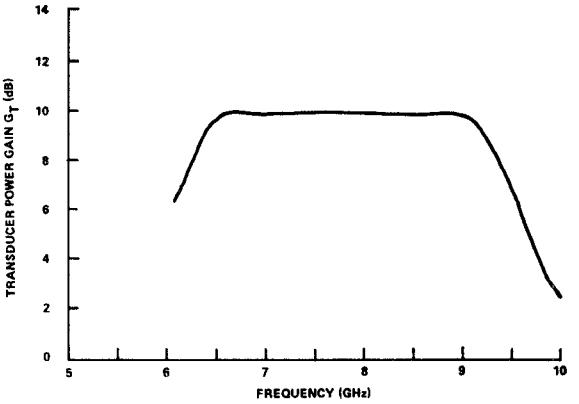

Fig. 9. Parametric amplifier response for the final design.

TABLE I

PRELIMINARY MATCHING NETWORK DESIGN FOR AN EQUIVALENT NEGATIVE RESISTANCE (R_{eq}) OF $-14\ \Omega$

Parameter	Value
C_A	0.4000
L_S	0.1000
L_A	0.7177
C_B	1.0820
L_B	0.3021
C_C	1.0960
L_C	0.2984
F_{pump}	34.3000

Note: Element values are given in nanohenries and picofarads. Transformer turns ratio is 0.8058:1.

TABLE II

FINAL MATCHING NETWORK DESIGN VALUES

Parameter	Value
C_A	0.4000
L_S	0.1000
L_A	0.7461
C_B	2.046
L_B	0.2240
C_C	0.5194
L_C	0.8707
F_{pump}	32.7000

Note: Element values are given in nanohenries and picofarads. Transformer turns ratio is 0.8058:1.

chosen and, for illustrative purposes, a circulator value of 25 Ω will be employed.

Proceeding with the first step in the design procedure outlined in Section III (Step 1 of Fig. 6), the computer-generated preliminary Butterworth[6] matching network design values are obtained. The equivalent circuit realization is presented in Fig. 7 and the corresponding element values are given in Table I.

[6] A preliminary design employing Chebyshev prototypes [24] has been found to yield less satisfactory results due to problems with convergence of the computerized optimization scheme.

If the preliminary design values given in Table I were employed in the amplifier realization, assuming that $X(\omega)$ is no longer negligible, the resulting response would appear as shown in Fig. 8.

Proceeding with Step 2 of Fig. 6, the preliminary matching network element values L_A, C_B, L_B, C_C, and L_C of Fig. 7 are adjusted automatically by the computerized synthesis technique to achieve a desirable flat gain response. The final amplifier response and corresponding element values which were obtained upon completion of this step are presented in Fig. 9 and Table II, respectively.

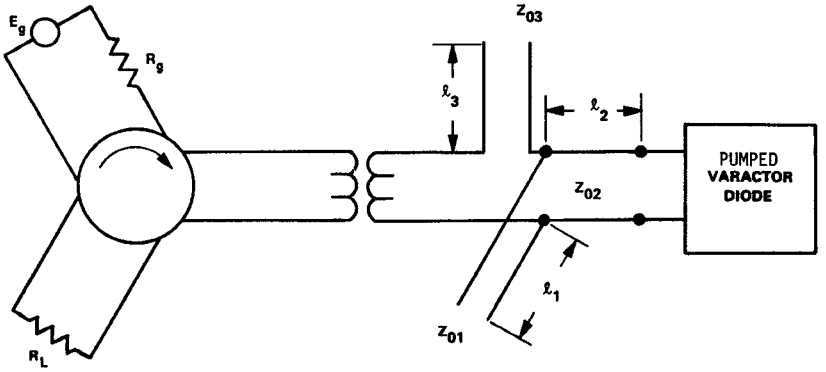

Fig. 10. Final amplifier design (see Table II for element values).

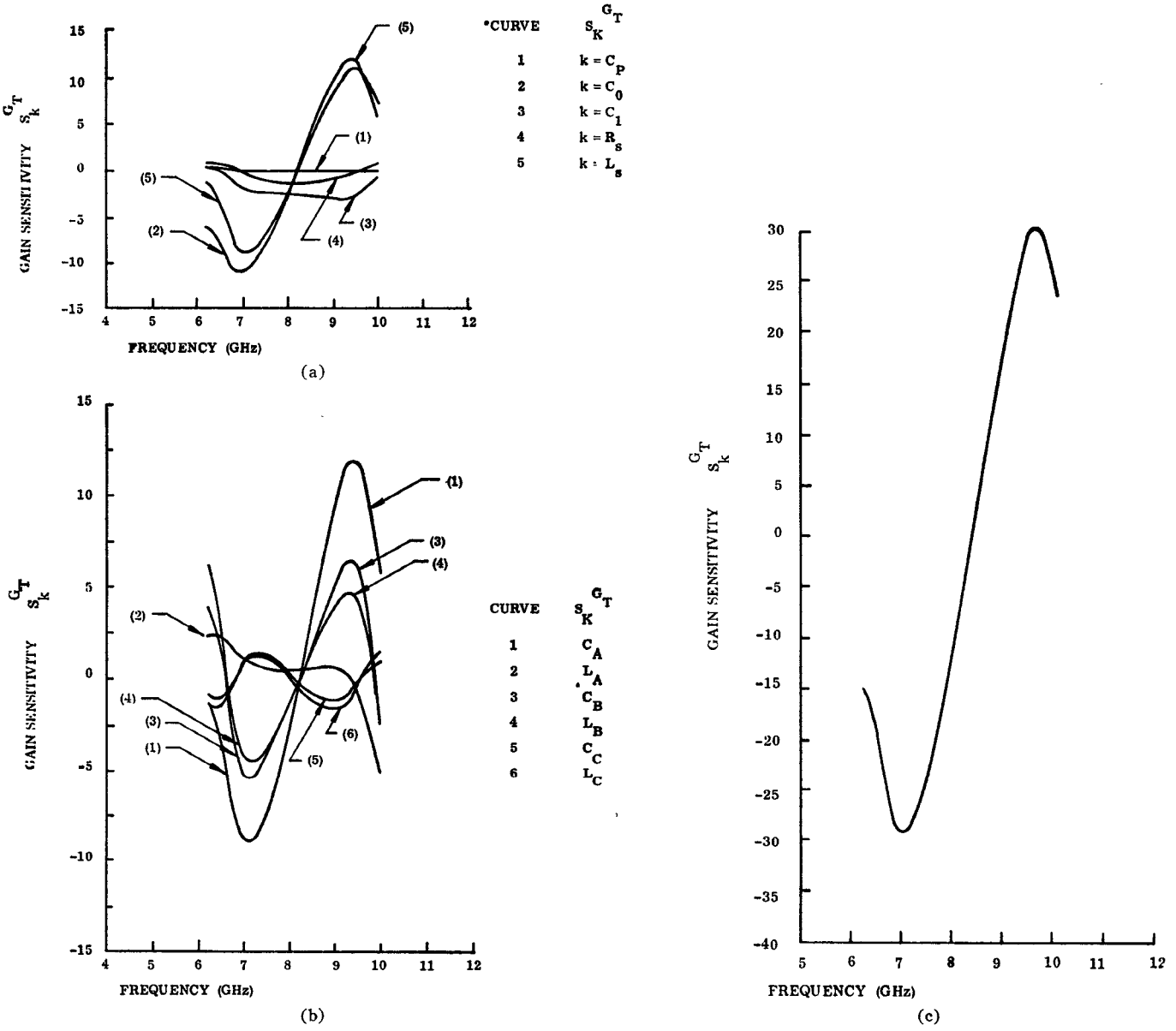

Fig. 11. (a) Amplifier sensitivity with respect to varactor diode parameters. (b) Amplifier sensitivities with respect to matching network parameters. (c) Amplifier sensitivity with respect to pump frequency.

TABLE III
ELEMENT VALUES FOR THE DISTRIBUTED REALIZATION

Transmission Line (cm)	Value (Ω)
Z_{01}	15.6700
1_1	1.9085
Z_{02}	120.0000
1_2	0.1997
Z_{03}	28.6000
1_3	1.9250

Employing standard techniques [28], the lumped matching network of Fig. 7 converts into the distributed realization shown in Fig. 10 and Table III.

It has been pointed out previously by numerous investigators [2], [5] that a parametric amplifiers' response is a hypersensitive function of its parameter values. Employing the definition of gain sensitivity given previously, Fig. 11(a), (b), and (c) exhibits quantitative data on the sensitivity of amplifier response to various parameters. Fig. 11(a) shows the sensitivity of the amplifier gain with respect to the diode parameters for the lumped-component amplifier realization. The obvious conclusion to be drawn from this data is that great care must be taken to accurately measure the varactor parameters. In particular, the zero pump frequency capacitance represented by C_o, and the diode series inductance L_s must be determined with great precision.

Fig. 11(b) and (c) are plots of the amplifiers sensitivity with respect to matching network parameters and pump frequency respectively. In general, the gain is most sensitive to parameter variations at the band edges. Of all the parameters for matching network M_s, it appears that capacitor C_B and inductor L_B (see Fig. 7) are most critical. For example, at 9.5 GHz, the gain sensitivity with respect to capacitor C_B, $S_{C_B}^{G_T} = 7$. This implies that for a 1 percent change in the design value for C_B, the transducer power gain will change 7 percent to 10.7 dB which constitutes a significant perturbation in the response; as illustrated in Fig. 11(c), the gain is most sensitive to slight changes in pump frequency.

V. CONCLUSIONS

The theory of broad-band nondegenerate parametric amplifiers was investigated in this paper. Employing the fundamental charge and voltage relations for a nonlinear capacitive junction, the matrix relation for a linear time-varying circuit model was written. From this relationship, a practical equivalent network for the varactor diode, including parasitics, was formed. The circuit for the complete parametric amplifier, including matching network, was then developed.

A mathematical synthesis technique was then formulated to provide a preliminary amplifier design. The complete preliminary amplifier realization was obtained from a prescribed Butterworth approximation utilizing closed formulas. The procedure for obtaining the final matching network element values was based upon the development of a viable optimization scheme.

To solve the problem of properly selecting the acceptable set of network parameters, the following steps were employed.

1) Determine the analytic expression for the amplifier response G_T in terms of its parameters values, select an appropriate objective function, and determine the initial values for the amplifier parameters from the preliminary matching network synthesis.

2) Compute the value of the objective function, determine whether its magnitude is within some previously determined value, and adjust the amplifier element values so that new values are obtained which will minimize the value of the objective function.

3) Repeat 2) until the objective function falls within some predetermined specification.

As a result of careful consideration of the analytical form of the nondegenerate parametric amplifier problem and after a certain amount of computer experimentation, the following steps were determined to yield the best design results.

1) Constrain the imaginary part of the active device impedance $X(\omega)$, to be zero.

2) Constrain the varactor package capacitance C_p to be zero.

3) Begin the optimization over a narrow band of frequencies, and continue to optimize the response over greater and greater bandwidths.

4) When the desired bandwidth is obtained, remove the constraint listed in 1) and optimize for the desired response [3].

5) Remove the constraint listed in 2) and optimize for the desired response.

By way of an example, the synthesis technique was shown to provide an excellent solution to the problem of obtaining broad-band amplifier designs.

As a bonus, the exact partial derivatives employed in the optimization may be used to compute the amplifier gain sensitivity with respect to all matching network and varactor diode parameters. Quantitative results indicate that amplifier performance is an extremely sensitive function of the pump frequency. The sensitivities with respect to the varactor diode parameters indicate that for effective design, great care must be taken in device characterization.

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An Octave-Band Switched-Line Microstrip 3-b Diode Phase Shifter

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***Abstract*—The design of an octave-band (2.5–5.0-GHz) switched-line diode phase shifter is described. An analysis showing the need for a choice of the shunt-diode switch configuration for broad-band operation is presented. Curves of even- and odd-mode impedance of parallel coupled microstrip lines employed in Schiffman differential phase shifters are presented. The configuration and performance characteristics of the phase shifter are described.**

I. Introduction

IN A RECENT PAPER [1], it was concluded that microwave switched-line diode phase shifters employing coupled transmission-line elements of the type described by Schiffman [2] were limited in bandwidth to about 1/2 octave. It was further stated that this bandwidth limitation occurs because the effective length of the off transmission path becomes a multiple of a half-wavelength in the frequency band of interest, where all incident power is reflected back to the generator.

In this paper, the off-path insertion loss of switched-line phase shifters employing both series- and shunt-configured diode switches is determined. It is shown that the bandwidth limitation described in [1] can be averted by use of the shunt configuration. The design of an octave-band switched-line 3-b microstrip diode phase shifter operating in the 2.5–5.0-GHz frequency band is presented. The performance characteristics of this phase shifter are also included.

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II. Effect of Switch Configuration on Phase-Shifter Performance

The two configurations that were considered for the phase shifter to be described are shown in Fig. 1. The configuration utilizing series diode switches was initially thought to be the most desirable because the position of the diodes relative to the input and output junctions does not impose a potential bandwidth limitation as it does in the shunt-diode switch case. However, analysis of a mathematical model of the configuration utilizing series switches revealed that it had operating points in the octave band at which the isolation between switching paths becomes very low. At these points, the phase-shifter insertion loss becomes very high and the phase error large. The configuration employing shunt diode switches was not found to have this problem. The problem was examined further by determining the insertion loss of the off transmission path (i.e., the path where maximum insertion loss is desired) [3]. The problem under consideration exists when some separation of good quality diodes is found to produce very low insertion loss in that path. This analysis is initiated by considering the two-port network having wave amplitudes a_1 and b_1 at port 1 and a_2 and b_2 at port 2, as shown in Fig. 2. The wave amplitudes at port 1 and port 2 are related using the cascading matrix T:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = T \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}. \quad (1)$$